

Multilevel Nonvolatile Memory by CMOS-Compatible and Transfer-free Amorphous Boron Nitride Film

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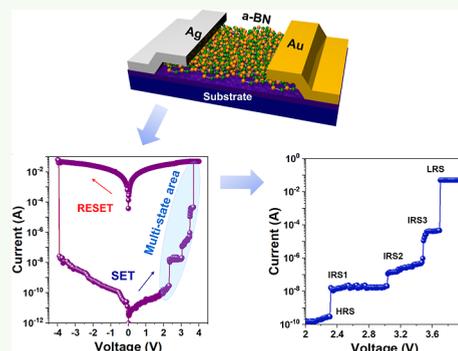
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ABSTRACT: Exploiting the multistate characteristic, we have engineered a single memristor based on amorphous boron nitride (a-BN) capable of rivaling the logic capacity of multiple field-effect transistors (FETs). The quintessence of our work is the realization of quinary resistive switching with five distinct resistive states enabled by a wafer-scale, chemical vapor deposition (CVD) grown a-BN thin film. This feat is achieved directly on the substrate, eschewing the need for transfer processes and leveraging low-temperature synthesis. The device exhibits an exceptional On/Off ratio of $\sim 10^8$, sustained over a significant cycling lifespan. We uncover the intricate interplay between the a-BN channel thickness and the quantized resistive states, revealing a precision-controlled resistive landscape. This capability addresses the production and transfer bottlenecks associated with two-dimensional materials, setting the stage for our a-BN-based memory device to advance the frontiers of ultrahigh-density data storage and computing systems.

KEYWORDS: amorphous boron nitride, resistive switching memory, multilevel memory, CMOS-compatible, chemical vapor deposition, intermediate resistive switching states



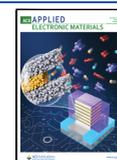
1. INTRODUCTION

Resistive switching memories (RSMs) have emerged as a superior alternative to traditional flash memories and random-access memories due to their high operating speed, enhanced device density, reduced cost, and significant nonvolatility.^{1–5} The challenge, however, lies in transcending inherent limitations and physical constraints to realize ultrahigh data storage capacities without compromising integration density.^{1,2} Addressing this, two strategies surface: reducing memory cell size and increasing the number of states per cell through multistate integration. While the former is laden with challenges including data processing issues,³ charge leakage,⁴ and fabrication complexities,⁵ the latter appears more viable by augmenting the levels between the “On” and “Off” states within each cell.

Sustainable and reproducible intermediate states have been achieved, capable of enduring numerous read-write cycles. These states can be reconfigured using structural and scale engineering techniques,^{5,6} significantly enhancing data storage capacity by transitioning from binary to multilevel memory states.^{1,7,8} Multilevel memories (MLMs) are poised to store multibit information per unit cell, thereby boosting storage capacity and reducing power consumption without aggressive downscaling.⁹ Beyond materials and fabrication, multiple conductance states are pivotal for improving computational precision in artificial neural networks (ANNs).¹⁰ For instance, a great deal of attention is paid to multiplication-addition accelerator and multilevel computing of RSMs specifically in reservoir computing (RC) as an important family of models in

neuromorphic systems.¹¹ Utilization of RSM characteristics memristors in the reservoir layer can enhance the efficiency of the computing system.¹² Typically, resistive switching in shared memories yields two outputs, “On” and “Off”, corresponding to binary states “1” and “0”. With n states, the data storage potential is $\log_2(n)$ bits. For example, a single cell with 32 distinct levels can store 5 bits, surpassing binary capacities. The future of ultrathin electronics and neuromorphic applications hinges on the compatibility of new materials with the demands for higher storage densities, continued miniaturization, and simplified device configurations. A high resistance On/Off ratio is crucial for stable multilevel resistive switching performance. For RSM-based artificial synaptic devices, it is essential to manage resistive switching through these intermediate states.¹³ Despite efforts to establish MLMs, the search for effective devices is hampered by a lack of suitable materials, apt device configurations, and switching principles. While various organic materials have been explored,^{14–18} achieving multistate reliability with inorganic memory channels remains challenging, with organic RSMs facing issues of low-density storage capacity,¹⁹ slow switching speeds, and long-term material instability.²⁰ Layered

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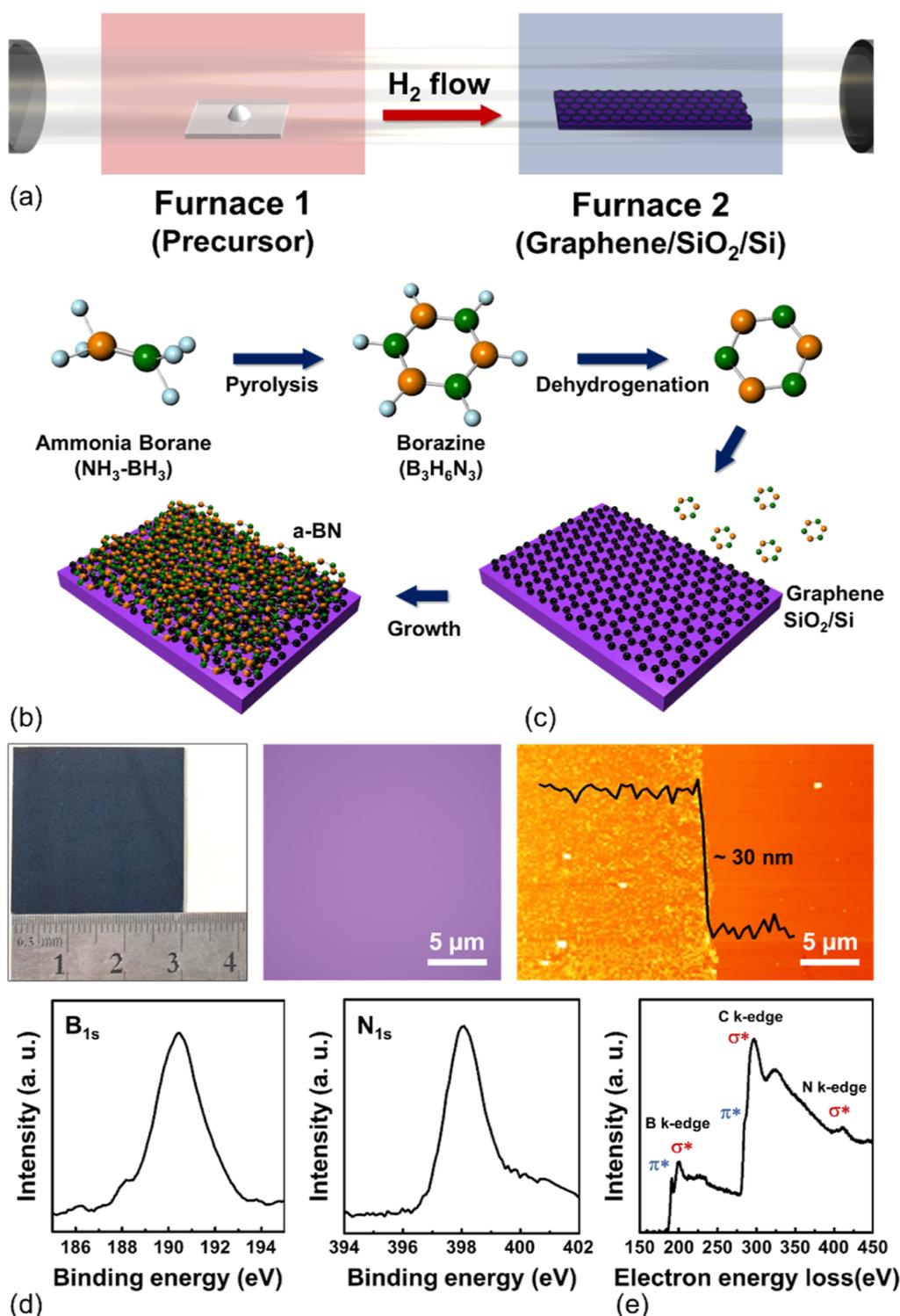


Figure 1. (a) Schematic illustration of double-zone low-pressure chemical vapor deposition system and growth mechanism of the a-BN film and (b) photo and optical microscope image of large-scale grown a-BN thin film on SiO₂ (inset), and (c) AFM image of surface morphology of a-BN thin film with 30 nm thickness, (d) XPS profiles for B_{1s} and N_{1s} peaks, and (e) electron energy loss spectroscopy (EELS) of the a-BN thin film.

materials with mono to few-layer structures have shown promise for ultrathin logic and memory devices, thanks to their atomic thinness,^{21–25} mechanical flexibility, low operating voltage, ease of surface engineering, and nonvolatile switching properties.^{26,27}

Multilevel resistive switching memory (MLRSM) devices have been fabricated with various two-dimensional (2D) materials.^{2,21,22,28,29} However, these often suffer from high

leakage currents³⁰ and poor environmental stability.³¹ Boron nitride, in contrast, exhibits exceptional physical properties, such as high mechanical strength and chemical stability, making it suitable for robust electronic^{32–36} and photonic devices.^{32,37,38} Metal/a-BN/metal devices, in particular, have shown significant binary RS performance, including high retention time,³⁹ excellent On/Off ratios,⁴⁰ and high write/erase cycling,^{41,42}

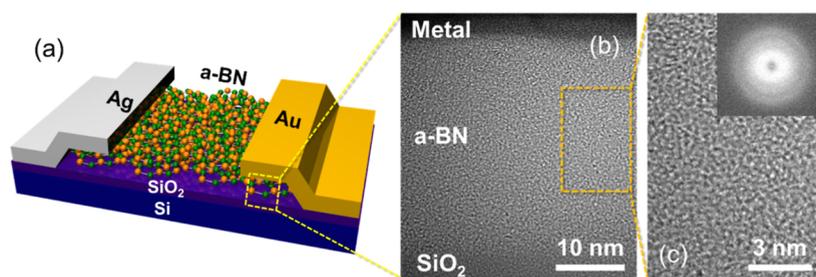


Figure 2. (a) Schematic illustration of a-BN MLM device, (b) HR-TEM image of the device, (c) high-resolution TEM image of a channel where inset shows diffraction pattern shows the amorphous structure of boron nitride.

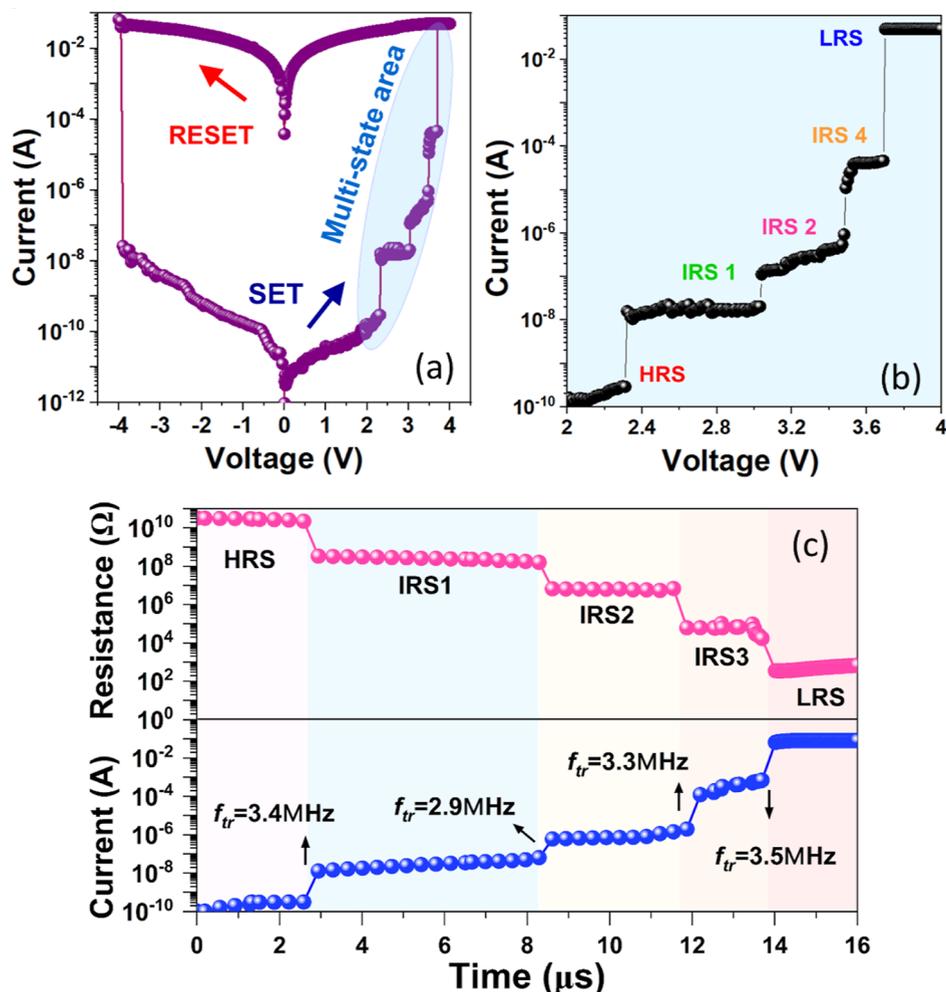


Figure 3. (a) I - V characteristic, (b) zoomed I - V characteristics with intermediates level states, (c) resistance (top) and current (bottom) switching over time among five states, and related transition frequency.

along with superior bending endurance.⁴⁰ Nevertheless, the challenge of high-temperature wafer-scale growth of h-BN⁴³ remains, especially considering the temperature sensitivity of CMOS circuits.⁴⁴ Additionally, most materials used in MLMs are not compatible with existing Si-based CMOS technologies, which is a barrier to the mass production of reliable devices. Therefore, 2D-material-based MLMs necessitate the development of transfer-free techniques and low-temperature growth conditions that are compatible with CMOS integration technology.

In this study, we propose a high-performance multilevel memory device based on wafer-scale and low-temperature

grown a-BN. Our device leverages a transfer-free growth approach, enabling direct integration of BN memory onto a substrate, circumventing common transfer challenges. We investigate the resistive switching mechanism, which is attributable to two primary factors: injected Ag ions and variations in metallic filament size and number. To our knowledge, this is the first report of a multilevel memory device implemented reliably in a 2-dimensional structure utilizing boron nitride materials.

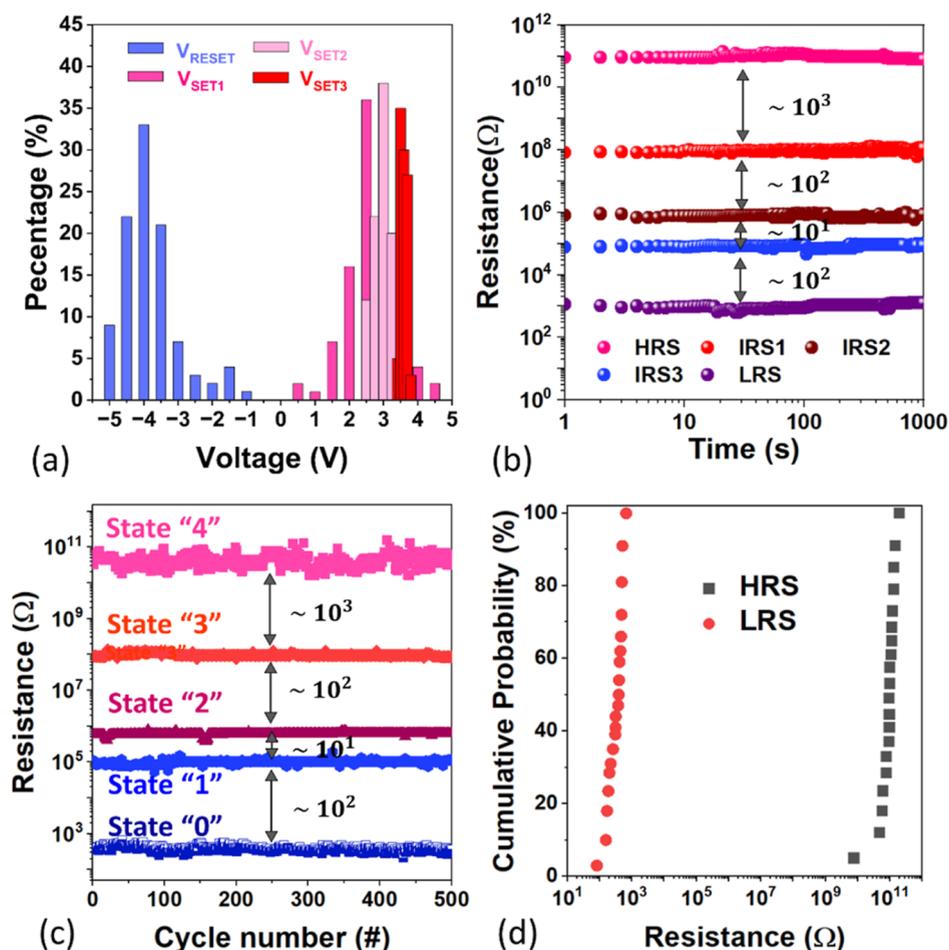


Figure 4. (a) The variations in V_{SET1} , V_{SET2} , V_{SET3} , and V_{RESET} , (b) retention performance with five resistance states (HRS, IRS1, IRS2, IR3, and LRS), (c) endurance performance with five different resistance levels, and (d) device-to-device uniformity of the resistance at LRS and HRS are collected from 20 a-BN memory devices.

2. RESULT AND DISCUSSION

2.1. Low-Temperature Growth of a-BN. The a-BN was synthesized using a two-zone low-pressure chemical vapor deposition (LPCVD), depicted in Figure 1a. The a-BN films were synthesized by the LPCVD method. A SiO_2/Si was used as a substrate following ultrasonic cleaning and O_2 plasma treatment. A borane–ammonia complex was the precursor used for a-BN deposition. The substrate and precursor temperatures during growth were 250 and 100 °C, respectively. Finally, transparent and centimeter-scale a-BN film is uniformly coated on the 300 nm SiO_2/Si substrate (see the Experimental Section).

Surface morphology and thickness of the grown a-BN thin film were determined using atomic force microscopy (AFM), as shown in Figure 1c. The height differential between the substrate and the a-BN film indicates a thickness of approximately 30 nm. We produced several a-BN thin films with thicknesses ranging from 3 to 30 nm, demonstrating uniformity across areas as large as several centimeters squared. This large-scale, direct CVD growth of a-BN thin films presents a promising route to circumvent the limitations associated with the high-temperature annealing required for atomic layer deposition (ALD) and CVD growth of hexagonal boron nitride (h-BN) at temperatures exceeding 400 °C.^{35,36} High-resolution X-ray photoelectron spectroscopy (XPS) scans of B_{1s} and N_{1s} peaks, displayed in Figure 1d, correspond to the individual

boron and nitrogen atoms, situated at binding energies of 398.3 and 190.6 eV, respectively. This confirms that the a-BN comprises sp^2 -bonded B and N atoms.⁴⁵ The peak shapes and positions suggest minimal contamination, while the absence of an oxidation peak typically found around 192.1 eV⁴⁶ signifies that the a-BN surface did not undergo oxidation. Electron energy loss spectroscopy (EELS) was utilized to map the distribution of B and N atoms in pristine a-BN, as demonstrated in Figure 1e. The identified around 200 and 411 loss peaks correspond to B and N, corroborating the formation of the BN film.

2.2. Memory Performance. The schematic of our fabricated Ag/a-BN/Au MLM device on the SiO_2 substrate is depicted in Figure 2a. A cross-sectional TEM image in Figure 2b confirms the a-BN layer's thickness at approximately 30 nm, sandwiched between the SiO_2 substrate and the Ag electrode, without discernible atomic ordering. Enlarged TEM images and the corresponding diffraction patterns (inset of Figure 2c) assess the atomic structure of the memory channel, corroborating the amorphous nature of the boron nitride thin film. This assertion is further supported by the intensity profile analysis of the back-folded edge, which indicates an average lattice spacing of 0.48 nm derived from electron diffraction data, characteristic of an amorphous structure (Figure S1, Supporting Information).

Differing thicknesses of a-BN thin films were deposited on SiO_2 substrates via LPCVD, upon which patterned drain and

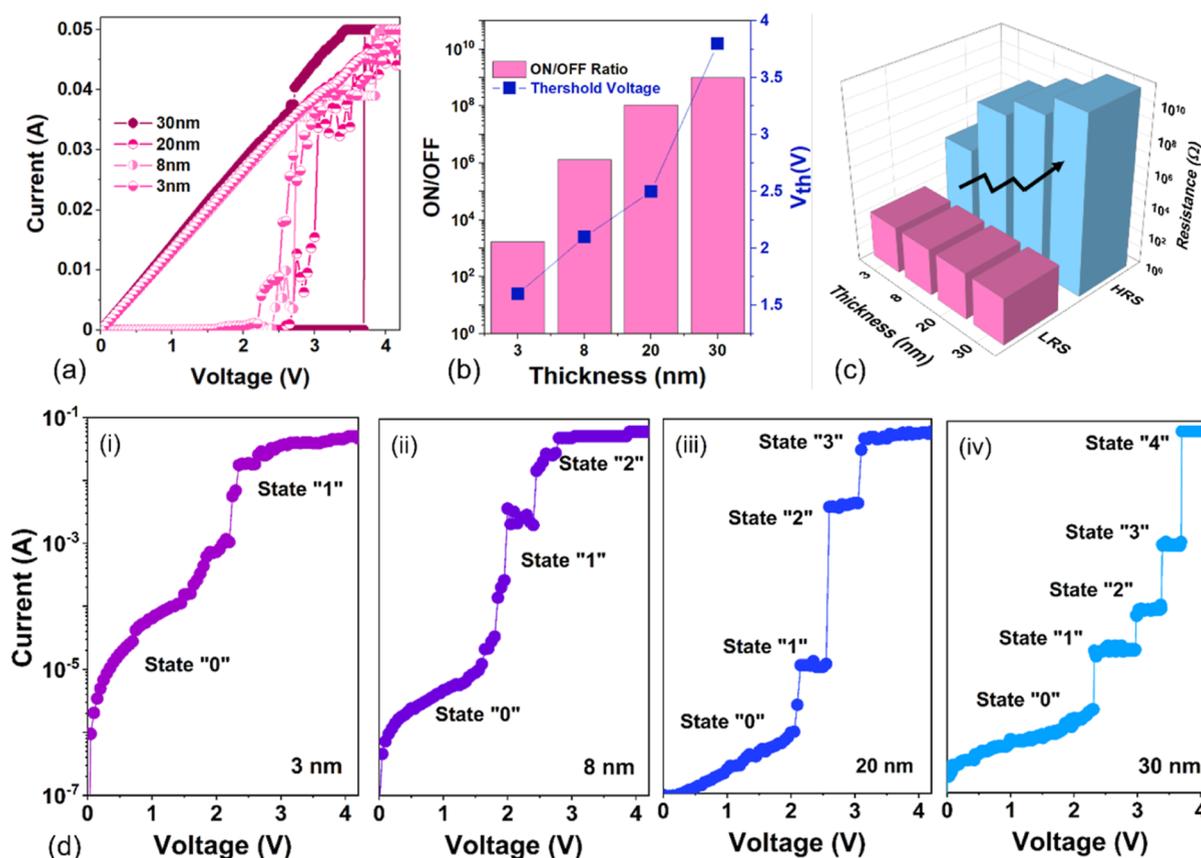


Figure 5. (a) Thickness-dependent I – V measurement, (b) On/Off current ratio and threshold voltage versus a-BN channel thickness of memory cell. (c) Variation and (d) number of intermediate states to the a-BN film thickness of (i) 3, (ii) 8, (iii) 20, and (iv) 30 nm.

source electrodes were established. The Ag and Au electrodes are 50 nm thick and deposited by thermal evaporation equipment. Our lateral a-BN MLM device, in contrast to vertically configured RS devices, can be modulated via multiple terminals. This lateral design facilitates versatile multiterminal signal input, enabling the emulation of neural functions for synaptic devices^{47,48} and applications in in-memory computing.⁴⁹ The electrical properties of the a-BN memory were appraised, with Figure 3a presenting the I – V characteristics for an RSM with a 30 nm channel. We want to note that our device has a dimension of $2.5 \times 4 \mu\text{m}$ (length \times width). Exhibiting stable bipolar resistive switching behavior, the device offers advantages for high-performance applications, particularly when leakage current is mitigated. During electroforming, the channel exhibits high resistance status (HRS), with bias voltage sweep starting at zero and extending to approximately 2.3 V, at which point a noticeable surge in current indicates a shift to the first intermediate resistive state (IRS1), coinciding with a significant reduction in resistance. Continued bias enhancement precipitates a second abrupt increase at a V_{SET} of 3 V, transitioning the memory to IRS2. Progressing to a V_{SET} of 3.6 V, the device attains a third intermediate state, IRS3, before settling into a low resistive state (LRS). This quintenary RS behavior encompassing HRS, IRS1, IRS2, IRS3, and LRS demonstrates the multilevel switching capability inherent to our a-BN RSM (Figure 3b). We denote the onset voltage transitioning from HRS to IRS1 as $V_{\text{SET}1}$. Also, we observed, the transition time from HRS to each of the intermediate states and LRS, as shown in Figure 3c. Transition starts with sudden resistance/current increase until a critical voltage reaches any of the threshold

voltages (e.g., $V_{\text{TIRS}1}$, $V_{\text{TIRS}2}$, $V_{\text{TIRS}3}$, V_{TLRS}) which is similar to the behavior raised by the conductive path rupture. The corresponding transition frequencies for each of the resistive states are stages 3.4, 2.9, 3.3, 3.5 MHz.

Figure 4a charts the consistency in peak $V_{\text{SET}1}$, $V_{\text{SET}2}$, $V_{\text{SET}3}$, and V_{RESET} values across multilevel SET and RESET cycles, illustrating precise control over HRS and LRS at corresponding SET and RESET voltages. The consistency of $V_{\text{SET}1,2,3}$ has been established, ensuring reliable RS behavior with uniformity in all SET and RESET voltages that surpasses that of high dielectric BN RSMs^{50,51} and organic RSM counterparts.^{52,53} An effective write/erase operation, considerable endurance, and a multilevel storage capacity are imperative for an optimal data storage system.⁵⁴ Figure 4b highlights the retention capabilities of our a-BN MLM, maintaining five discrete resistive levels across a duration of over 10^3 seconds. Resistance readings taken at 0.6 V demonstrate this noteworthy switching ratio, effectively countering the common issue of leakage current in typical 2D switching channels. Memory endurance over 500 cycles is exhibited in Figure 4c, identifying five discrete resistive levels with resistances spanning 10^3 to 10^{11} . These findings suggest that conducting filaments (CFs) are initially narrow, expanding progressively with incremental bias voltage, leading to intermediate expansion states and ultimately, a comprehensive CF facilitating a lower resistance path at LRS. The discernible resistance gaps between the states ensure minimal error potential during standard read/write operations, suggesting these five distinct states as a foundation for BN-based ultrahigh-density data storage.

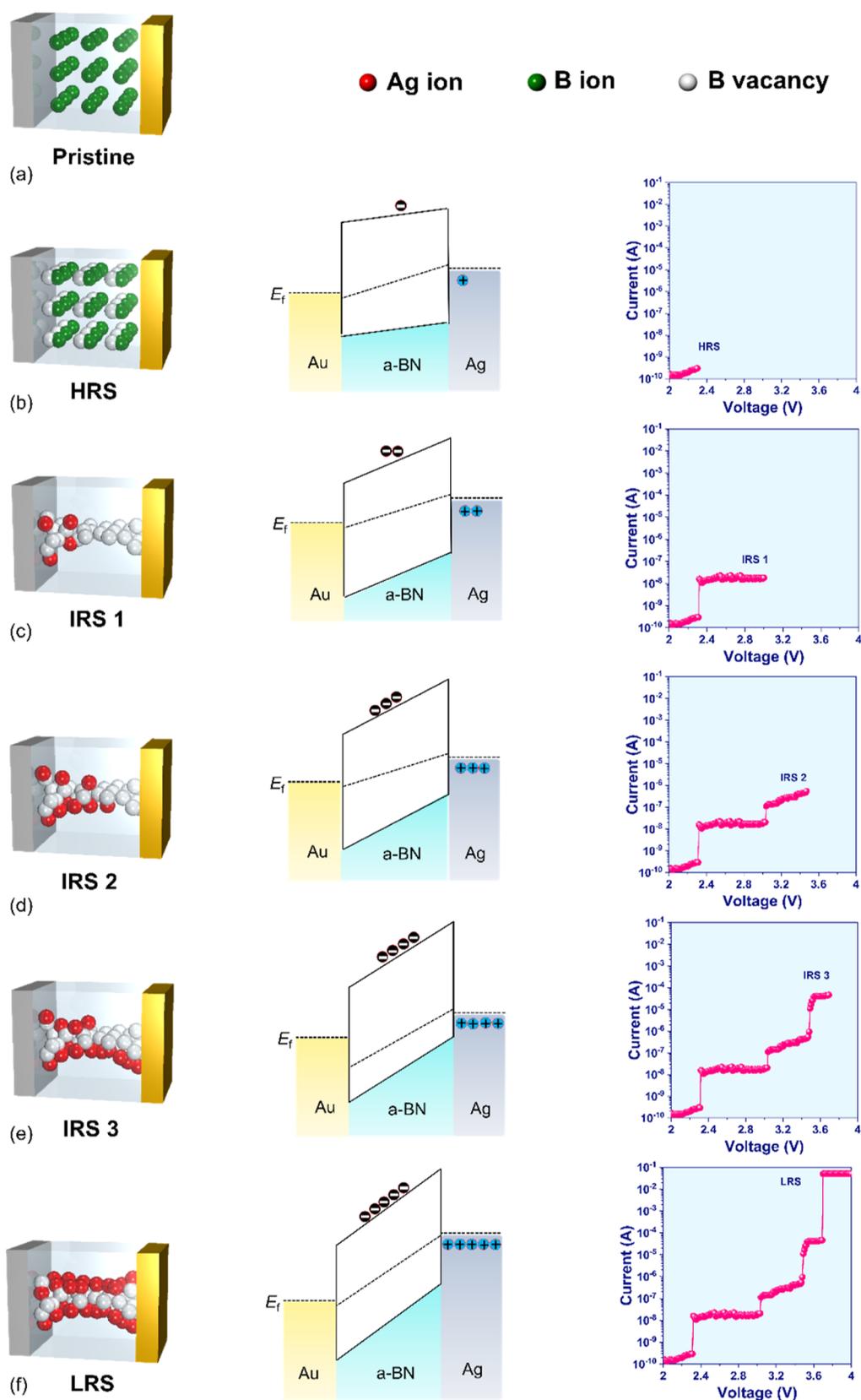


Figure 6. Schematic illustration of the contribution of metal ions and vacancies generation and growth of conducting filaments which results in RS, energy band diagram, and corresponding $I-V$ characteristics for (a) pristine, (b) HRS, (c) IRS1, (d) IRS2, (e) IRS3, and (f) LRS.

Uniformity across devices is paramount for the reliability of memory systems. We evaluated this by analyzing the switching performance across several devices and observed a narrow LRS

and HRS resistance distribution spanning over 8 orders of magnitude, as detailed in Figure 4d. The cumulative probability data for each resistance state of a set of 20 cells were performed.

Additionally, we investigated the influence of a-BN film thickness on resistive switching (RS) behavior, with results indicating a substantial impact, shown in Figure 5a. The On/Off ratio improves significantly as the channel thickness increases, illustrated in Figure 5b,c, due primarily to a decrease in HRS for thicker a-BN films. A thinner a-BN layer, containing a greater amount of diffused Ag, shows a decreased On/Off ratio in contrast to thicker layers, where Ag diffusion is less prominent.⁵⁵ The dependency of multilevel RS on thickness is demonstrated in Figure 5d. As the a-BN layer thickness increases, intermediate states surface between HRS and LRS, and their number rises with increased thickness, likely due to the necessity for higher biases to accumulate Ag ions and establish conductive pathways to the electrode. On the other hand, no intermediate state was observed for $t = 3$ nm where the memory device directly switched from HRS to LRS. However, for $t = 8, 20,$ and 30 nm, one, two, and three intermediate states emerged, respectively and the voltage positions of state one and state two shifted to higher voltages. Furthermore, for $t = 20$ and 30 nm, the third intermediate state (state 3) has formed, where this peak has also shifted to upper voltages with increasing channel thickness. This shift is because the diffusion barrier cannot completely break through the thicker channel to form a connection pass between two electrodes leading to higher local V_{SET} and a new intermediate level (state 3). Also, we compared our device performance with the state-of-the-art BN-based memories,^{37,39–41,50,51,56–59,65–68} our fabrication process holds significant advantages in terms of growth temperature, applicability to CMOS integration, and device performance.^{60–62,64}

2.3. Mechanism of Resistive Switching. Our investigations into the a-BN-based RSM have identified four principal conduction mechanisms and energy band diagrams within a 30 nm thick a-BN device, as illustrated in Figure 6. At relatively low bias voltages, Ag ions migrate toward the electrode by creating boron vacancies within the a-BN channel. These vacancies, with lower formation energy than nitrogen vacancies, serve as traps for Ag ions, facilitating the formation of conductive paths. At the same time, the current remains subdued, adhering to the Ohmic conduction regime (segment 1).⁶³ Also, the energy band diagram shown in the middle column shows the initial state, a barrier layer formed by a-BN has a blocking effect on the electron transport, and the memory device is at HRS. As the forward bias increases the band alignment at the interfaces tilts the energy band of a-BN, consequently modulating the energy barrier [697]. Where B ions start to migrate and related doping is generated. Upon increasing the bias voltage beyond 2.3 V, the HRS transitions to an intermediate resistive state (IRS), characterized by additional ion trapping and conductive pathway formation. The enhanced doping generated by trapped ions, further electrons in the conduction band of a-BN shown in the band diagram (see Figure 6c). This low voltage does not suffice for ions to diffuse through the channel fully where the negative ions are further created through the a-BN channel (Figure 6d). This leads to the manifestation of IRS, governed by trap-controlled space charge limited conduction (SCLC), evident as a sharp rise in current (segment 2). As the bias crosses 3 V, the trapping of Ag ions escalates, achieving a state of trapped charge-limited current (TCLC) conduction around a V_{SET} of 3.4 V. This progression culminates in the switch to the LRS. Reversing the bias from +3.5 V back to 0 V prompts boron ions to return to their vacancies, reverting the channel to HRS

through Ohmic-like conduction (segment 4). The memory's endurance, demonstrated at a read voltage of 0.6 V in Figure 4c, showcases stable HRS and LRS for numerous cycles, with an On/Off resistance ratio of approximately 10^8 and durable endurance beyond 500 cycles. The resistance retention over time, measured at 0.6 V for both HRS and LRS, confirms the longevity of the states (Figure 4c). The emergence of each intermediate state at distinct voltages results from the inception or alteration of filament size, altering channel resistance. Distinct from HRS, the LRS exhibits less dependency on the channel area due to the filamentary nature of conduction when the memory is active (Figure 3a). Interface-type conduction, known for its size-dependent behavior,⁶⁹ may not significantly influence our memory device's operation. The presence of water molecules trapped at the interface between a-BN and the SiO₂ substrate could potentially introduce trap sites, contributing to the multilevel switching observed.

3. CONCLUSION

In summary, our work presents a multilevel resistive switching device based on a-BN, showcasing intermediate states and delineating the operational mechanisms and characteristics. The multibit memory performance is marked by high endurance, an extensive On/Off ratio, and stable retention throughout the forming period. The device stably maintained all five resistive states for at least 500 cycles, with exceptional uniformity observed across multiple devices. The number of intermediate states notably depends on the a-BN film's thickness, which underpins the multistate switching behavior due to the evolution of filament dimensions within the channel. Our implementation of low-temperature, direct growth of a-BN-transfer-free on a substrate is a pivotal step toward addressing temperature incompatibility and transfer challenges, advancing wafer-scale integration of 2D materials with CMOS technology.

4. EXPERIMENTAL SECTION

4.1. Material Growth. A 300 nm SiO₂/Si substrate was positioned in the growth zone (furnace II) following ultrasonic cleaning and O₂ plasma treatment. Subsequently, a borane–ammonia complex (NH₃–BH₃, 97% purity, 10 mg, Sigma-Aldrich) was introduced into the precursor zone (furnace I) for a-BN deposition. The substrate and precursor were heated to 250 and 100 °C, respectively, under a pressure of approximately 110 Torr, with a hydrogen (H₂, 99.999%) flow of 22 sccm. After reaching the target a-BN film thickness, the furnaces were cooled to room temperature to halt the growth, and the samples were extracted. Figure 1b displays a centimeter-scale a-BN film uniformly coated on the 300 nm SiO₂/Si substrate. A corresponding inset showcases the transparent a-BN film coverage.

4.2. Material Characterizations. HR-TEM analyses were taken using Seron AIF 2100 and Philips CM30. The surface morphology of the analyses was characterized by optical microscopy and Park NX10 AFM (Park System). The Raman spectroscopy (Alpha300 M+, WITec GmbH) with an excitation wavelength of 532 nm and laser power of 5 mW is used to investigate crystal properties of a-BN samples. The elemental composition of films was investigated by X-ray photoelectron spectroscopy (XPS) analysis (ESCA2000 spectrometry).

4.3. Device Fabrication. RSM devices with the structure of Ag/a-BN/Au on SiO₂ were fabricated with different a-BN channel thicknesses. The electrode configuration was determined by a shadow mask with an electrode area of 30 × 30 μm. The metal deposition process was performed to fabricate Ag and Au electrodes on top of the a-BN thin film using the thermal evaporator facility.

4.4. Device Characterization. A 4-probe setup connected to Keithley 2400 was used to determine the electrical characteristics of

Ag/a-BN/Au memory devices at room temperature under ambient conditions.

■ ASSOCIATED CONTENT

SI Supporting Information

The Supporting Information is available free of charge at <https://pubs.acs.org/doi/10.1021/acsaelm.4c01042>.

TEM images, lattice spacing of a-BN, comparison table for device performance and fabrication techniques (PDF)

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Notes

The authors declare no competing financial interest.

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