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Rigorous Study on Hump Phenomena in Surrounding Channel Nanowire (SCNW) Tunnel Field-Effect Transistor (TFET)

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Abstract: In this paper, analysis and optimization of surrounding channel nanowire (SCNW) tunnel field-effect transistor (TFET) has been discussed with the help of technology computer-aided design (TCAD) simulation. The SCNW TFET features an ultra-thin tunnel layer at source sidewall and shows a high ON-current (I_{ON}). In spite of the high electrical performance, the SCNW TFET suffers from hump effect which deteriorates subthreshold swing (S). In order to solve the issue, an origin of hump effect is analyzed firstly. Based on the simulation, the transfer curve in SCNW TFET is decoupled into vertical- and lateral-BTBTs. In addition, the lateral-BTBT causes the hump effect due to low turn-ON voltage (V_{ON}) and low I_{ON}. Therefore, the device design parameter is optimized to suppress the hump effect by adjusting thickness of the ultra-thin tunnel layer. Finally, we compared the electrical properties of the planar, nanowire and SCNW TFET. As a result, the optimized SCNW TFET shows better electrical performance compared with other TFETs.

Keywords: nanowire; TFET; subthreshold swing; low-power, steep switching; ultra-thin tunnel region; vertical band-to-band tunneling

1. Introduction

A reduction of power density in complementary metal-oxide-semiconductor (CMOS) technology becomes one of the major concerns as the CMOS devices have been scaled down [1], [2]. A tunnel FET (TFET) has been attracted as a substitutable device for an ultra-low power logic circuit since it can achieve subthreshold swing (S) less than 60 mV/decade at room temperature which allows TFET to be operated with the lower supply voltage (<0.5 V) maintaining a high ON-OFF current ratio (I_{ON}/I_{OFF}) [3–6]. However, experimental results have demonstrated that the TFET suffers from some critical issues such as low-level I_{ON}, ambipolar current and poor S [7,8]. There are several studies to address them with the help of narrow band gap materials [9–11], abrupt doping profile [12] and novel geometrical structures [13–15]. Among these studies, many papers propose a TFET with an ultra-thin tunnel layer at source sidewall which enables band-to-band tunneling (BTBT) perpendicular to the channel direction (vertical-BTBT) [16–23]. It can improve I_{ON} as well as S with the help of a large BTBT junction area and a short tunnel barrier width. However, it only considers a vertical-BTBT and ignores the other BTBT component including a BTBT parallel to the channel direction (lateral-BTBT), [24,25]. Since BTBT at sharp source corner is deeply related to the hump effect which degrades average S and I_{ON}, it should be examined rigorously for a device design optimization [26]. Therefore, more precise

analysis are required considering both vertical- and lateral-BTBTs in technology computer-aided design (TCAD) simulation [27–30].

This paper is composed as follow. First of all, device design parameters and TCAD simulation conditions for a gate-all-around (GAA)-NW TFET with an ultra-thin tunnel layer at source sidewall are explained. Second, after examining the basic operation of studied TFET, a fundamental origin of hump effect is analyzed by two-dimensional (2D) contour plots. Third, the influences of geometrical parameters on hump effect are investigated and analyzed to minimize undesired effect which degrades switching performance. Last of all, the optimized structure is compared with the control devices.

2. Device Fabrication

The device structure used in this work is similar to that in [16], except a lateral channel direction considering the compatibility with the state-of-the-art CMOS technology for a sub-5 nm-technology nodes [31] (Figure 1). It is named as a surrounding channel nanowire (SCNW) TFET, since its intrinsic (or lightly doped) channel which is named as tunnel region surrounds conventional nanowire structure. All the materials except for gate oxide are Si. The gate oxide is SiO_2. In TCAD simulation, a channel length (L_{CH}) is set by 30 nm to exclude short-channel effect. Considering the latest CMOS technology, a nanowire radius except surrounding channel (i.e., tunnel region) (T_B) and a gate oxide thickness (T_{OX}) are set by 7 nm and 1 nm, respectively. The other important design parameters are summarized in Figure 1 and Table 1. All the parameter variations in this simulation are set in consideration of the fabrication processes [32,33]. The following models are used for an accurate simulation result: Shockey-Read-Hall recombination, doping and field dependent mobility, and dynamic non-local BTBT after calibration by referring [17]. Since the thickness of tunnel region (T_{TUN}) is less than 8 nm, modified local density approximation is also used to consider quantum effect. In addition, the physical characteristics for BTBT is reflected by the calibrated current model based on the fabricated device [34–37]. For the calculation of BTBT generation rate (G) per unit volume in uniform electric field, Kane's model is use as follows:

$$G = A\left(\frac{F}{F_0}\right)^P \exp\left(-\frac{B}{F}\right), \tag{1}$$

where $F0$ = 1 V/m, P = 2.5 for indirect BTBT, A = 4.0 × 1014 $cm^{-1}{\cdot}s^{-1}$, and B = 1.9 × 107 $V{\cdot}cm^{-1}$ are the Kane's model parameters and F is the electric field [34]. The pre-factor A and the exponential factor B parameter are calibrated by referring [17].

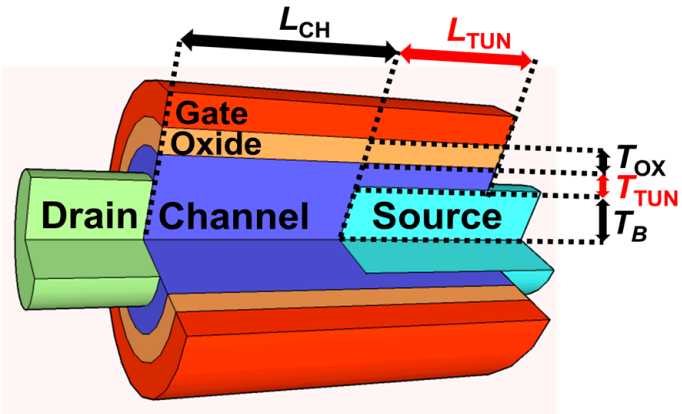

Figure 1. Schematic structure diagram and definitions of design parameters in SCNW TFET.

Table 1. SCNW TFET design parameters used for TCAD simulation.

Parameters	Value
Source doping concentration, *p*-type (N_S)	10^{20} cm^{-3}
Drain doping concentration, *n*-type (N_D)	10^{20} cm^{-3}
Body doping concentration, *p*-type (N_{CH})	10^{17} cm^{-3}
Gate work function	4.05 eV
Channel length (L_{CH})	30 nm
Nanowire radius except tunnel region (T_B)	7 nm
Gate oxide thickness (T_{OX})	1 nm
Length of tunnel region (L_{TUN})	Variable
Thickness of tunnel region (T_{TUN})	Variable
Drain voltage (V_{DS})	0.5 V

3. Hump Effect in SCNW TFET

Figure 2 shows drain current (I_D) versus gate voltage (V_{GS}) curves with 2 nm-T_{TUN} and 0.5 V-drain voltage (V_{DS}) while L_{TUN} is varied from 20 to 60 nm. The I_{ON} is extracted at 2.0 V-V_{GS} and 0.5 V-V_{DS}. The I_{ON} increases linearly proportional to the L_{TUN} which confirms that the BTBT junction area of SCNW TFET is determined by the L_{TUN}. Generally, the FETs based on a NW channel have a disadvantage for enhancing current drivability, which can be achieved by increasing a NW radius or using a multi-channel structure [38]. On the other hand, SCNW TFET can easily adjust I_{ON} by controlling a L_{TUN}. However, as shown in Figure 3a, there is a hump in the subthreshold region of SCNW TFET. The transfer curves are simulated with various V_{DS} values. At all the V_{DS} values, the hump current appears. In addition to this, with the higher the doping concentration, the better the ON-current is shown however, the hump effect is noticeable from 5×10^{19}-N_S cm^{-3} as shown in Figure 3b. The hump effect should be addressed for TFET's low-power application since it deteriorates average *S* which results in the degradation of I_{ON}/I_{OFF} and/or supply power (V_{DD})-scaling. Therefore, optimization for other parameters is needed to achieve high ON-current and hump-less transfer curve. In order to analyze the cause of hump effect, the electron BTBT generation rates (e^{BTBT}) are examined by 2D contour plots with different V_{GS} conditions (Figure 4). When V_{GS} is applied near a turn-ON voltage (V_{ON}), defined as V_{GS} when BTBT starts to occur, a lateral-BTBT is predominant. As V_{GS} increases, a vertical-BTBT starts to occur at 0.4 V-V_{GS} and finally surpasses the lateral-BTBT at 1.2 V-V_{GS}. Therefore, the current of SCNW TFET can be decoupled into two different BTBTs. In addition, transfer curves with various L_{TUN} are plotted in Figure 5. The I_D at low V_{GS} (< 0.9 V) is unchanged regardless of L_{TUN}, while I_D increases with longer L_{TUN} at high V_{GS} (> 0.9 V). The V_{GS} at this point is defined as hump voltage (V_{HUMP}). Since the tunnel junction area of vertical-BTBT component is only affected by L_{TUN}.

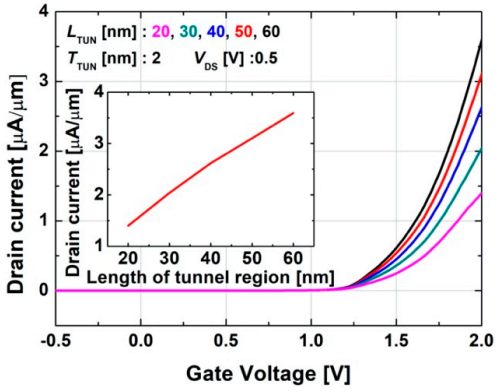

Figure 2. (Simulation) I_D-V_{GS} curves of SCNW TFET with 2 nm-T_{TUN} and 0.5 V-V_{DS} depending on the L_{TUN}. The inset shows I_{ON} as a function of L_{TUN}. For the SCNW TFET, the I_{ON} increases proportional to L_{TUN}.

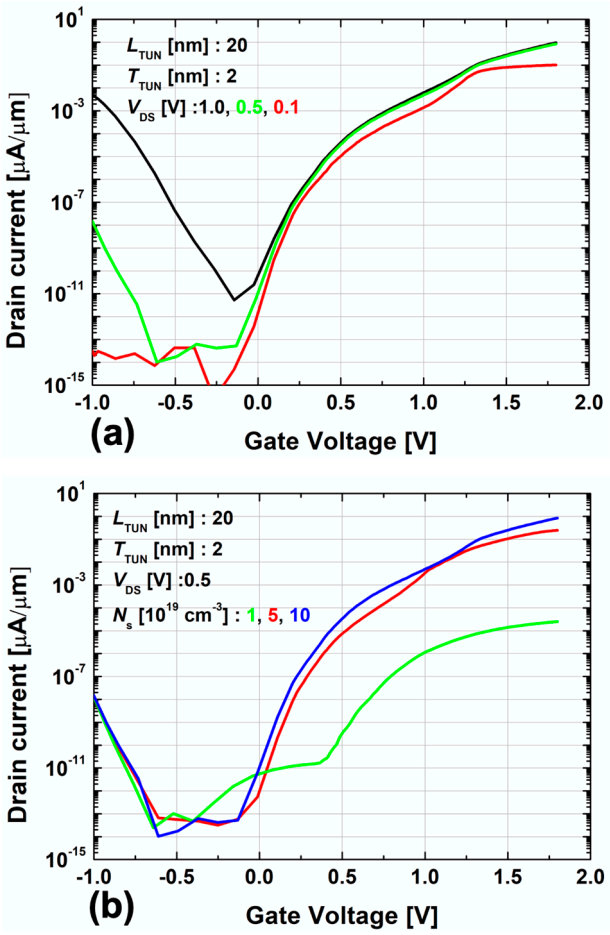

Figure 3. (Simulation) Log(I_D)-V_{GS} curves of SCNW TFET depending on the (**a**) V_{DS} (**b**) N_S. In spite of changing V_{DS} and N_S, the hump effect still remains.

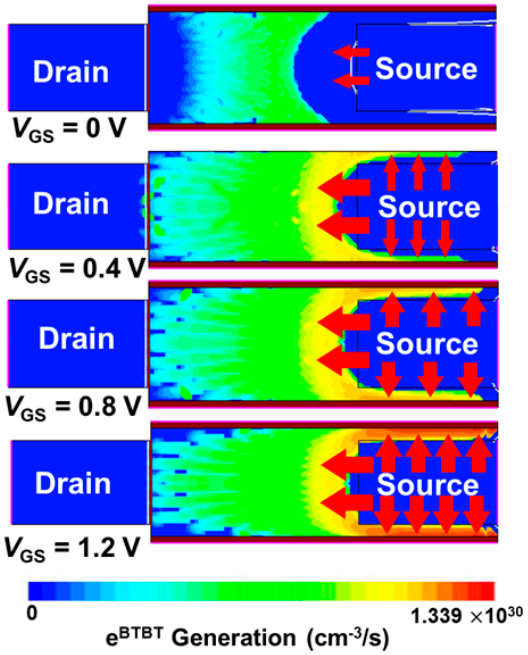

Figure 4. (Simulation) e^{BTBT} of SCNW TFET as V_{GS} increases from 0 to 1.2 V with 0.4 V step. T_{TUN} = 2 nm, L_{TUN} = 20 nm, and V_{DS} = 0.5 V.

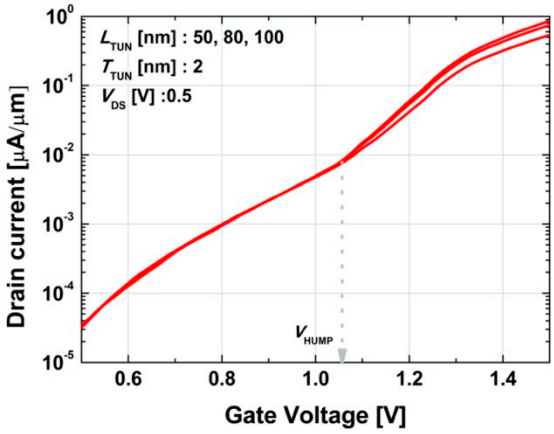

Figure 5. (Simulation) Log(I_D)-V_{GS} curves of the SCNW TFET when the L_{TUN} varies between 50, 80 and 100 nm.

4. Device Optimization

In Section 3, we confirmed that the hump behavior in SCNW TFET is mainly attributed to the two BTBT paths (i.e., vertical and lateral) which have different V_{ON} and BTBT rates. Therefore, a design optimization is needed to achieve maximum electrical performance (low S and high I_{ON}). In this Section, the influences of L_{TUN} and T_{TUN} on SCNW TFET's electrical characteristic are investigated since the vertical-BTBT mostly occurs in the tunnel region. Figure 6a shows transfer curves with 50, 80, 100 nm of L_{TUN} and 2, 3, 4, 5 nm of T_{TUN}. As shown in the inset of Figure 6a, the V_{HUMP} is clearly decreased as T_{TUN} increases. The results can be quantitatively analyzed and calculated by voltage division model in which the gate oxide and depletion capacitors (C_{ox} and C_{Si}) are connected in series (Figure 6b) [13]. Since T_{TUN} is ultra-thin (< 10 nm) and source is highly doped, it can be assumed that the tunnel region is entirely depleted; the C_{Si} is constant. Therefore, surface potential (ψ_S) is expressed as (2), where ε_{Si} and ε_{ox} are permittivity of Si and SiO_2, respectively. If T_{TUN} increases, ψ_S becomes large and vertical-BTBT occurs with the smaller V_{GS} which results in the decrease of V_{HUMP} as discussed in Figure 6a.

$$\psi_s = \frac{C_{ox}}{C_{ox}+C_{si}} V_{GS} = \frac{\frac{\varepsilon_{ox}}{T_{ox}}}{\frac{\varepsilon_{ox}}{T_{ox}}+\frac{\varepsilon_{Si}}{T_{tun}}} V_{GS} = \frac{1}{1+3\frac{T_{ox}}{T_{tun}}} V_{GS}\psi_s = V_{GS} - \frac{3T_{ox}}{T_{tun}+3T_{ox}} V_{GS}, \text{ where } \varepsilon_{Si} \approx 3\varepsilon_{ox} \quad (2)$$

Figure 7 shows transfer curves with various T_{TUN} from 2 to 8 nm, where L_{TUN} and V_{DS} are fixed at 20 nm and 0.5 V, respectively. According to the results, the I_D is clearly increased, and S is deteriorated as T_{TUN} becomes thinner. It is attributed to the enhanced vertical-BTBT rate with the smaller T_{TUN}, because the tunnel resistance (i.e., tunnel barrier width) of SCNW TFET is geometrically determined by the T_{TUN} [39]. However, an aggressive scaling-down of T_{TUN} is contradictory to the process capability and the S which gets worse as the T_{TUN} decreases due to an increased V_{HUMP}. Consequently, an optimization of T_{TUN} can be a strategy for SCNW TFET to compensate its weakness (i.e., low I_{ON} and hump effect) and/or enhance its strength (i.e., under 60 mV/dec-S at room temperature). Finally, T_{TUN} is optimized as 4 nm. Then, the performances of planar TFET, SCNW TFETs and nanowire TFET are compared. Figure 8a shows the average subthreshold swing (S_{avg}) and point-to-point minimum subthreshold swing (S_{min}) of SCNW, nanowire and planar TFETs. The S_{avg} is defined as the average inverse slope of the transfer curve while I_D changes from 10^{-12} μA/ μm to 10^{-2} μA/ μm. For S_{min}, the planar TFET, SCNW TFETs and nanowire TFET show similar values, all of which are less than 60 mV/dec. For S_{avg}, SCNW TFET shows the lowest value. Figure 8b shows transfer curve of planar TFET, SCNW TFETs and nanowire TFET. For fair comparison, the I_{OFF} of these devices should be adjusted to the same level. The above adjustment is achieved by changing the work function and channel doping concentration. The adjusted I_{OFF} is 10^{-7} μA/μm, referring to actual I_{OFF} in nanowire TFET [40]. The Figure 8b shows that the SCNW TFET has a larger I_{ON} than that of the planar and

nanowire TFETs. In detail, its I_{ON} is enhanced 2.4 times more than that of nanowire TFET and 4.7 times more than that of planar TFET. In addition, the SCNW TFET shows higher I_{ON} than other devices at 0.53 V-V_{GS} and fully operates within 0.7 V-V_{GS}.

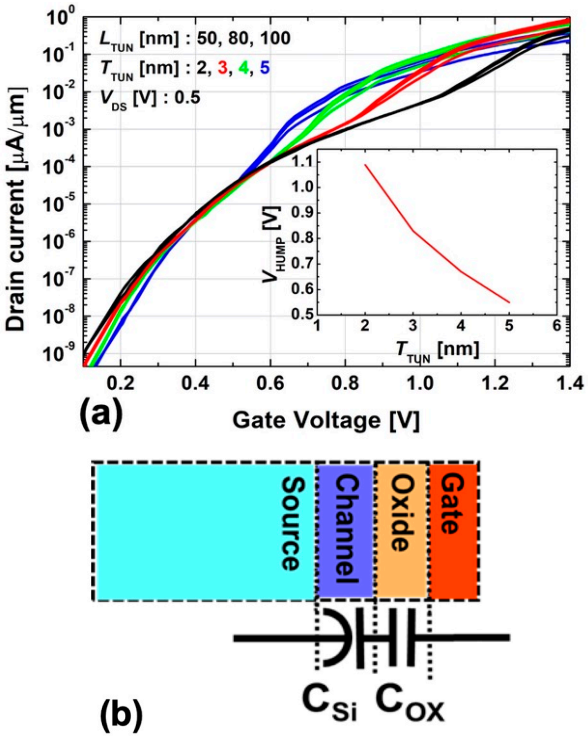

Figure 6. (Simulation) (**a**) Log(I_D)-V_{GS} curves of SCNW TFET according to T_{TUN} with the various L_{TUN}. The inset shows that the V_{HUMP} is clearly decreased as T_{TUN} increases. (**b**) (Calculation) The capacitance model in the area of SCNW TFET where vertical-BTBT occurs.

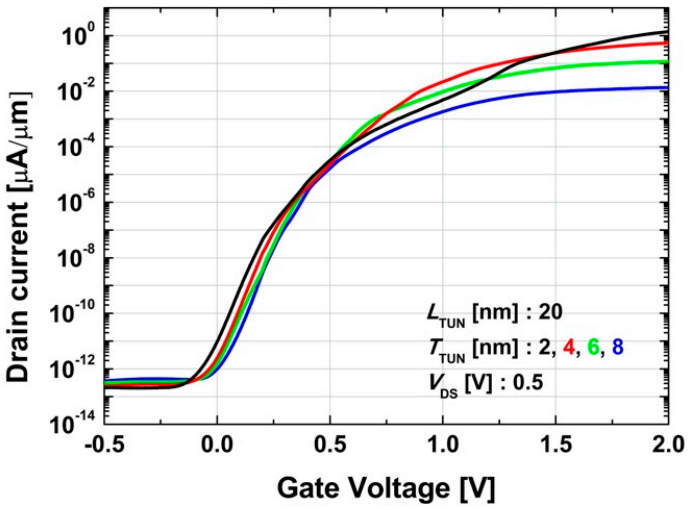

Figure 7. (Simulation) Log(I_D)-V_{GS} curves of the SCNW TFET with various T_{TUN}. The hump effect appears clearly, and S is deteriorated as T_{TUN} becomes thinner.

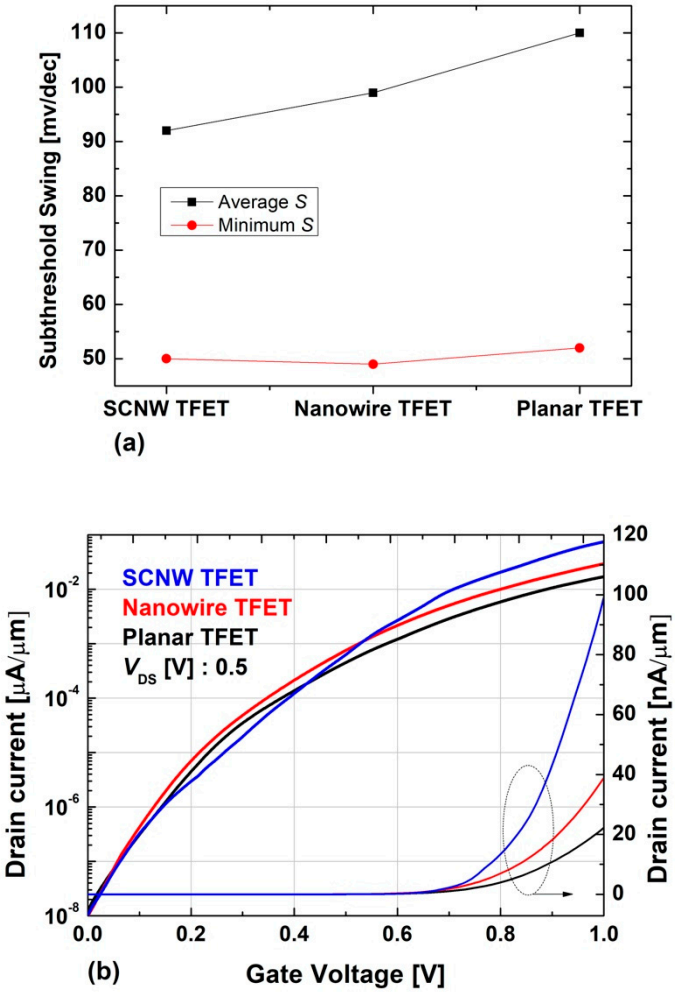

Figure 8. (Simulation) (**a**) S_{avg} and S_{min} (**b**) I_D-V_{GS} curves of planar TFET, SCNW TFETs and nanowire TFET.

5. Conclusions

The SCNW TFET has been studied for high electrical performance. It features nanowire TFET with a thin tunnel layer at source region. Based on the simulation, the transfer curve in SCNW TFET is analyzed and decoupled into vertical- and lateral-BTBTs. The vertical-BTBT is attributed to excellent I_{ON} rate and S. However, the lateral-BTBT causes the hump effect due to low V_{ON} and low I_{ON}. Therefore, the design optimization is suggested to reduce the hump effect and achieve maximum electrical performance (low S and high I_{ON}). Finally, the electrical performance without hump effect is optimized by adjusting the thin tunnel layer. In future work, novel design strategy to reduce lateral-BTBT will be suggested to eliminate the hump effect.

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