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Reducing the Optical Reflectance of Kerf-Loss Free Silicon Wafers via Auto-Masked CF_4/O_2 Plasma Etch

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Kerf-loss free (KLF) silicon can significantly contribute to the cost competitiveness of solar cells by reducing the amount of material wasted as the kerf loss during sawing process. Different techniques to produce KLF silicon wafers have been therefore studied, however, the fabrication processes for high efficiency solar cell with KLF wafers need further research. Since one of the major factors that decides the cell efficiency is the optical reflectance, the surface modification step such as anti-reflection coating or surface texturing process is necessary. In our experiment, auto-masked CF_4/O_2 plasma etching was used to obtain textured silicon surface with reduced reflectivity. As the bias voltage of CCP mode was varied, the morphology and the etch rate of the plasma-etched KLF silicon wafers were investigated. The reduction in the measured reflectivity demonstrated the effectiveness of the auto-masked texturing process on a KLF silicon wafer. These results will eventually attribute to providing cost-effective silicon solar cells.
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Silicon-based technology is the mainstream in photovoltaics industry since the solar cell production is currently based on silicon and the price of the wafers is the dominant factor in determining the total fabrication cost of the cells.[1] Most silicon wafers are made by multi-wire slicing process.[2] Although this technique has gone through substantial improvements, there are still several issues to be solved. One of them is the inevitable kerf-loss which is critical since it can increase up to ~70% as the thickness of wafers decreases.[2] This causes large material inefficiency, which is closely related to the cost of the cells. Kerf-loss free (KLF) silicon wafers are greatly advantageous in this respect. Unlike the wafers produced by the conventional slurry sawing process, KLF silicon can be produced into thin and ultra-thin wafers without the loss of the material (silicon). Therefore, various KLF wafering technologies in gas, liquid or solid phase have been actively studied as alternatives to the costly sawing process.[3] Pinto et al. investigated a gas phase wafering method, silicon dust sheet process, and it produces silicon ribbons through chemical vapor deposition from silane.[4] Most commercialized KLF wafers are prepared by liquid phase wafering method, such as ribbon growth on substrate, as it allows mass production through faster deposition rates.[5] Direct film transfer method demonstrated by Henley et al. corresponds to the solid phase wafering that uses ion beam-induced cleaving.[6] However, the fabrication techniques that are applicable to KLF wafers have not been explored yet. The particularity of polycrystalline KLF wafers including the brittleness and the low thickness needs to be considered when applying the process that has been developed for the conventional (poly)crystalline silicon wafer.

Reducing the reflectivity loss from silicon surfaces is an important issue in fabricating high efficiency solar cells. Coating antireflection (AR) layers is one of the major means to improve light trapping and decrease the optical reflectivity from the surface.[7,8] By controlling the refractive index of the coating layer, the destructive interference of light minimizes the reflection.[9] However, the use of hetero-materials can limit the thermal stability and eventually the long-term reliability. Different intrinsic thermal expansion property of each material can cause delamination between layers over time when exposed to the variation of the temperature. The geometrical texturization of the surface is another way of improving light absorption of the solar cells. The surface can be textured through either wet- or dry-etching.[10,11] The disadvantages of wet etching include less freedom in choosing the substrate and the substantial amount of chemicals used, therefore more chemical wastes produced. The plasma-based dry-etching is considered to have some distinctive advantages over wet-etching.[12] It can be applied to silicon independent of its crystallinity or prior treatment. Less toxic chemicals are used in the plasma etching process, which is fully compatible with the advanced microelectronic fabrication process. Hadobás et al. used interference lithography followed by reactive ion etching to prepare nanostructured silicon surfaces and observed a clear decrease in the optical reflectance when the depth of the structure increased.[13] Huang et al. combined self-assembled nanosphere lithography and photo-assisted electrochemical etching to form nanostructures with high aspect ratio and it successfully reduced the reflectance of silicon surface.[14] The nanopatterning of the silicon surface is an effective light harvesting technique, however, it usually includes complicated and costly lithography steps for mask preparation. By producing auto-masking particles during plasma etching process, the requirement of additional mask can also be solved.[15–17] In a controlled SF_6/O_2 atmosphere, auto-masking layer (SiF_xO_y) can be formed.[18–21] It is known that the passivating layer, SiF_xO_y, forms when the oxygen threshold is reached; the oxygen threshold varies depending on the etching conditions, especially the temperature.[22] The competition between the protection of masking layer and Si etching produces silicon nanostructures with high aspect ratio.[21,23] Although low temperature is preferred for the formation of masking layer, Gaudig et al. also made attempts to produce black silicon structure at room temperature.[24]

In our experiment, the surface of polycrystalline KLF silicon wafers were masklessly nano-textured through capacitively coupled plasma (CCP) etching system using CF_4 and O_2 gases. The morphology of nanopillars created on silicon surfaces were controlled by varying the DC bias voltage. The resulting surface composition after the plasma etching process was also analyzed by using X-ray photoelectron spectroscopy (XPS). The reflectance spectra of the nano-textured silicon surfaces under different bias voltages confirmed the effects of the maskless CF_4/O_2 plasma etching on the reflection properties of KLF silicon substrates.

Experimental

Auto-masked plasma etching for surface texturing of a KLF silicon wafer was performed in a plasma system, which can be operated in a mode of either inductively coupled plasma (ICP) or CCP. In the ICP mode, a plasma is ignited by applying a 13.56 MHz radio-frequency (RF) source power to an induction coil. Another 13.56 MHz RF bias power is independently applied to an electrode, where the source power controls the plasma density while the bias power controls the ion energy. In the CCP mode, only bias power is applied to the electrode to generate the plasma. Thus, the bias power affects both density and energy of the ions in the CCP mode. In this study, auto-masked plasma etching was conducted in the CCP mode. Each polycrystalline KLF

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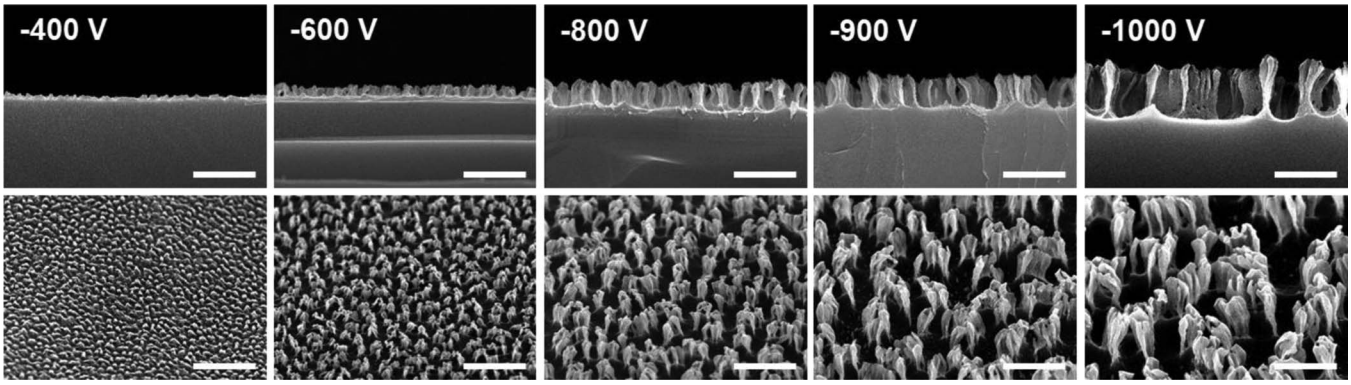

Figure 1. SEM images of textured KLF silcon substrates after plasma etching at bias voltage of −400, −600, −800 and −1000 V. The top and bottoms rows are the cross-section and tilted view of SEM images, respectively. (scale bar: 1 μm).

silicon wafer was prepared in the size of 10 × 10 mm^2. The plasma etching was performed under CF_4 and O_2 flow rates of 30 and 25 sccm, respectively, and the pressure in the reaction chamber was 50 mTorr. The bias power to the electrode was varied in the range of 40–300 W, resulting in the DC bias voltage ranging from −400 to −1000 V. Each sample was etched for 20 min.

The morphological analysis was made using field emission scanning electron microscopy (FE-SEM, JEOL, S-4800) under the acceleration voltage of 15 kV. The optical properties were examined through the reflectance spectra in the wavelength range of 200–800 nm obtained by a UV-Vis spectrometer (Jasco, V-650). Surface compositional analysis was carried out by XPS (Thermo Electron, K-Alpha), which had the X-ray source of 1486.6 eV generated from a moveable Al node at 15 kV.

Results and Discussion

In the presence of SF_6/O_2, the fluorine radicals react with silicon to etch it by forming volatile SiF_4 while the ionized products SiF_y^+ react with oxygen radicals to form silicon oxyfluoride, SiO_xF_y.[23] This layer is treated as an inhibitor when simply etching silicon, however, this auto-masking behavior can also be exploited to reduce the reflectivity of silicon surface and fabricate black silicon.[25] Previous reports on silicon surface texturing through auto-masked (or maskless) plasma etching was mainly based on SF_6/O_2 plasma. The use of CF_4 also allows etching of Si through similar reactions; fluorine radicals etch silicon surface, and the addition of O_2 to the CF_4 plasma leads to the formation of SiO_xF_y layer. Unlike SF_6/O_2 plasma, CF_4/O_2 plasma induces the formation of fluorocarbon films on SiO_xF_y layers during surface texturing. When a substrate (Si, SiO_2, Si_3N_4, etc.) is exposed to fluorocarbon plasmas like CF_4, thin steady-state fluorocarbon films form on the surface of the substrate as a result of simultaneous deposition and consumption of fluorocarbon films, which can also act as an etch-inhibitor.[26] It is expected that Si surfaces coated with fluorocarbon films and SiO_xF_y are more etch-resistant. Therefore, CF_4 was chosen instead of SF_6 to effectively protect silicon surfaces from further etching by fluorine radicals in the texturing process.

The SEM images (Figure 1) show the evolution of the morphology of KLF silicon substrates resulting from the surface texturization as the bias voltage is varied from −400 to −1000 V. SEM images were obtained from the cross section (top row) and tilted view (bottom row) to get three-dimensional information of the nanostructures. By using CCP and injecting O_2 gas in CF_4 plasma etching, the silicon surface was etched anisotropically to form nanopillar structures as shown in SEM images (Figure 1). As mentioned above, the use of CF_4/O_2 plasmas results in Si surfaces partially covered with fluorocarbon films as well as SiO_xF_y layers while the unprotected Si surfaces are etched anisotropically. SiO_xF_y layers and fluorocarbon films are also known to passivate the sidewalls of silicon structures, therefore helps maintaining the shape of the pillars with high aspect ratio. The random and dense nanopillars formed at a low bias voltage of −400 V can be seen in the tiled SEM image. The height of the nanopillars is still small probably because the etching process has stopped at its initial stage. With increasing bias voltage, the heights of the nanopillars increase as clearly seen in the cross-section images (top row of Figure 1). This is caused by the increase in the etch rate as the bias voltage increases. Furthermore, the nanopillars agglomerate together as the average distance between the nanopillars increase with increasing magnitude of bias voltage as shown in the tilted SEM images (bottom row of Figure 1). In fluorocarbon plasmas, ion-assisted chemical etching is a major contributor to silicon etching. As higher etch rate proceeds etching deeper and increase the roughness, the trenching effect may have occurred. This effect removes the passivating layer in

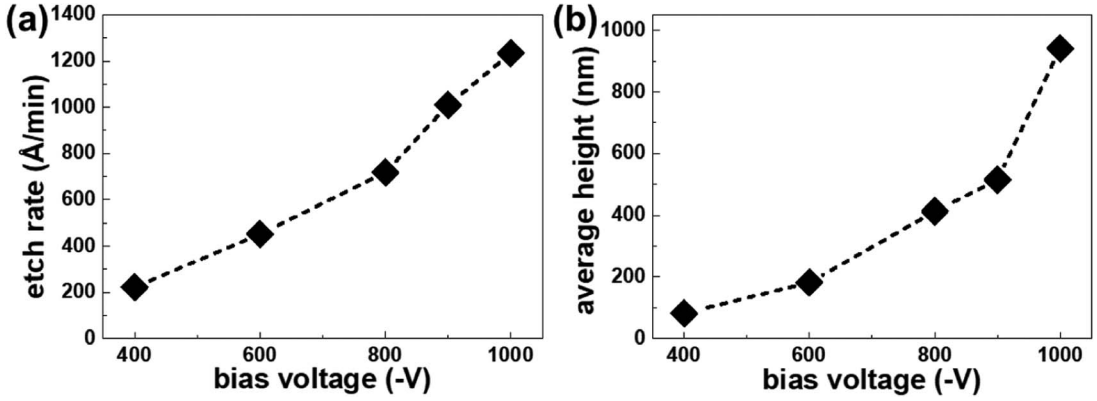

Figure 2. (a) Etch rate of KLF silicon and (b) the average height of silicon nanopillars as the bias voltage is varied from −400 to −1000 V.

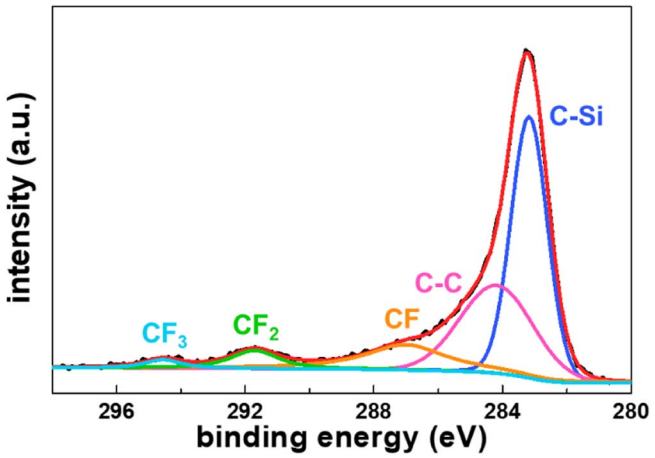

Figure 3. XPS spectrum of KLF silicon substrate after plasma etching at bias voltage of −1000V.

the valleys faster and finally exposes the silicon underneath. Therefore, silicon is more likely to be etched anisotropically once the structure of pillars is formed. As SiO_xF_y layer is less stable and can dissociate at elevated temperatures, a continued etching may cause local heating of the substrate and the valleys will be etched vertically and horizontally due to the exothermic reaction of fluorine etching.

The measured etch rate of KLF silicon and the average height of the pillars depending on the bias voltage are demonstrated in Figures 2a and 2b, respectively. As discussed above, the etch rate increases with increasing magnitude of bias voltage. The etch rate starts from ∼222 Å/min at −400 V bias and reaches ∼1,234 Å/min at −1000 V bias. As the bias voltage was varied from −400 V to −1000 V, the average height of pillars ranged from ∼82 to ∼941 nm. The height of nanopillars seems relatively short considering the etch rate as the formation of auto-masking layer is required to initiate the fabrication of nanopillars. Thus in the beginning stage of etching, a relatively uniform etching over the silicon surface would take place. Also, the masking layer may not perfectly protect silicon underneath during the whole etching process; SiO_xF_y layer may dissociate when heated or attacked by ion bombardments. The ratio of height of nanopillars to the etched thickness of substrate is generally higher for increased etch rate, which is consistent with the trenching effect mentioned above because the etch rate in the valleys is faster than at the top surface of pillars.

The formation of the fluorocarbon films under a CF_4/O_2 plasma was confirmed by XPS measurements. Figure 3 shows the XPS spectrum of carbon 1s obtained from the silicon surface textured by auto-masked plasma etching at a bias voltage of −1000 V. The XPS peaks at ∼284.2, ∼287.0, ∼291.7, and ∼294.5 eV are assigned to C-C, C-F, $C-F_2$, and $C-F_3$, respectively, implying that the fluorocarbon films are formed on the silicon surface in a CF_4/O_2 plasma.[27,28]

The optical reflectance as a function of wavelength was measured for bare and textured KLF silicon as shown in Figure 4a. The optical reflectance of the textured surfaces is significantly reduced compared to that of the bare silicon surface, especially in the UV/visible range. As the valleys between the nanopillars grow laterally and vertically, the optical reflectance is further decreased due to the light trapping effect.[14,29] The nano-textured surface has different influence on the optical reflectance depending on the wavelength of the incoming light. The multi-scattering effect is effective in reducing the reflectance in short wavelengths. The gradual change in the refractive index of the textured region of the silicon surface can also suppress the surface reflection in the long wavelengths. The refractive index of a bare silicon substrate would change abruptly at the surface of the substrate. As a consequence of the surface texturing, the change in the refractive index would become gradual since the average refractive index of the nanostructures would lie in between those of the atmosphere and KLF silicon.[30,31] The change in the optical reflectance was quantitatively compared using the weighted mean reflectance (R_w), obtained by Eq. 1, where $S_{AM\ 1.5\ G}$ is the AM (Air Mass) 1.5 G solar spectral irradiance, and R(λ) is the reflectance of the nano-textured KLF silicon samples.[32]

$$R_W = \frac{\int_{300\,nm}^{800\,nm} R(\lambda) S_{AM1.5G}(\lambda) d\lambda}{\int_{300\,nm}^{800\,nm} S_{AM1.5G}(\lambda) d\lambda} \quad [1]$$

Figure 4b shows that R_w was ∼32% for bare Si and decreased to ∼14% after auto-masked plasma etching at a bias voltage of −1000 V. Generally, the optical reflectance of the nano-textured silicon surface was reduced as the magnitude of bias voltage during plasma etching was increased.

Conclusions

Auto-masked plasma etching of a KLF silicon wafer was investigated in order to reduce its optical reflectance through surface texturing. CF_4/O_2 plasma was used in a CCP mode and the bias voltage was varied to effectively control the properties of silicon nanostructures, which were etched masklessly into a form of nanopillars with different sizes due to auto-masking layers. As the magnitude of bias voltage was raised from −400 to −1000 V, the etch rate and the average height of the nanopillars were increased from ∼222 to ∼1,234 Å/min and from ∼82 to ∼941 nm, respectively. Beside a SiO_xF_y layer, fluorocarbon films were formed on the surface of silicon and contributed to auto-masking behavior. The optical reflectance of KLF silicon samples were significantly reduced as the light trapping effect was enhanced; R_w was reduced by ∼56% when bare silicon was

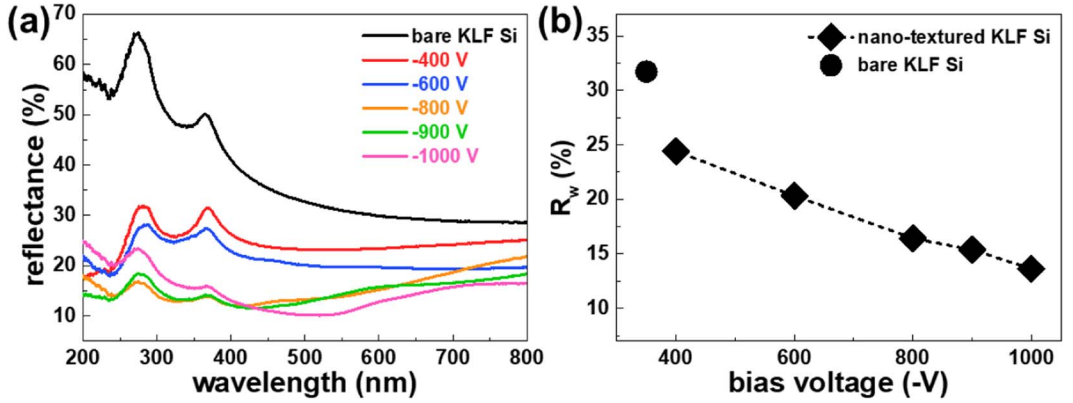

Figure 4. (a) Optical reflectance vs. wavelength of bare and nano-textured KLF silicon under varying bias voltage. (b) The weighted mean reflectance obtained from the optical reflectance in (a).

etched at −1000 V. The application of auto-masked surface texturing using a CF_4/O_2 plasma etching can take KLF silicon-based solar cell technology a step further toward commercialization.

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